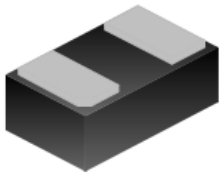
PESDMC2FD5VB

Bi-directional 5V Low Capacitance ESD Protector

Description

The PESDMC2FD5VB protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, low operating voltage. It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.



DFN1006-2L(Bottom View)

Feature

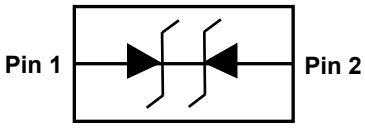
- 40W peak pulse power per line (t_P = 8/20μs)
- DFN1006-2L package
- Replacement for MLV(0402)
- Bidirectional configurations
- Response time is typically < 1ns
- Low clamping voltage
- RoHS compliant
- Transient protection for data lines to
  IEC61000-4-2(ESD) ±15KV(air), ±15KV(contact);
  IEC61000-4-4 (EFT) 40A (5/50ns)

B1

Marking (Top View)

Applications

- Cellular phones
- Portable devices
- Digital cameras
- Power supplies



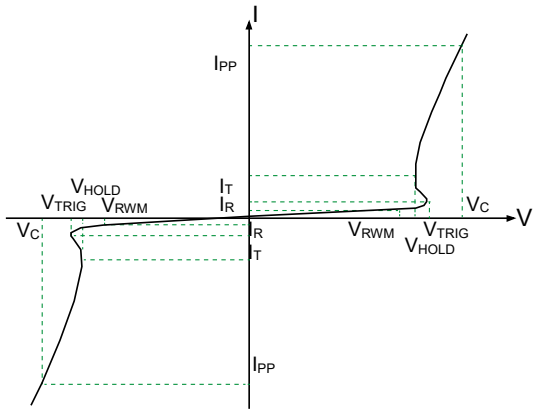
Circuit Diagram

Mechanical Characteristics

- Mounting position: Any
- Qualified max reflow temperature:260℃
- Device meets MSL 1 requirements
- DFN1006-2L without plating

Electronics Parameter

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{TRIG}	Reverse trigger Current
V_{HOLD}	Reverse holding voltage
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electrical characteristics per line@25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Peak Reverse Working Voltage	V_{RWM}				5.0	V
Reverse trigger voltage	V_{TRIG}	I_{TRIG}=30mA	8.0	9.2	10.5	V
Reverse holding voltage	V_{HOLD}	I_{HOLD}=60mA	6.0	7.0	8.0	V
Reverse Leakage Current	I_R	V_{RWM} = 5V T=25℃			1.0	μA
Maximum Reverse Peak Pulse Current	I_{PP}			4.2		A
Clamping Voltage	V_{CL}	I_{PP}=16A t_p=100ns		15.6		V
Clamping Voltage	V_C	I_{PP}=1A		8.8	9.2	V
Clamping Voltage	V_C	I_{PP}=3A		9.2	9.5	V
Clamping Voltage	V_C	I_{PP}=4A		10	11	V
Junction Capacitance	C_j	V_R=0V f = 1MHz		0.42	0.5	pF

Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (t_p=8/20μs)	P_{pp}	40	W
Operating Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃

Typical Characteristics

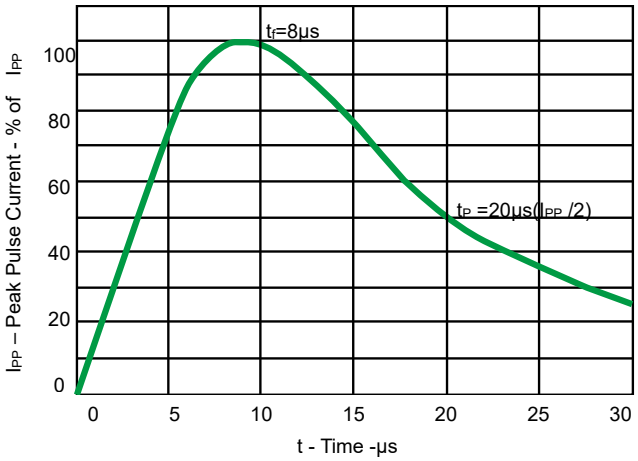


Fig 1.Pulse Waveform

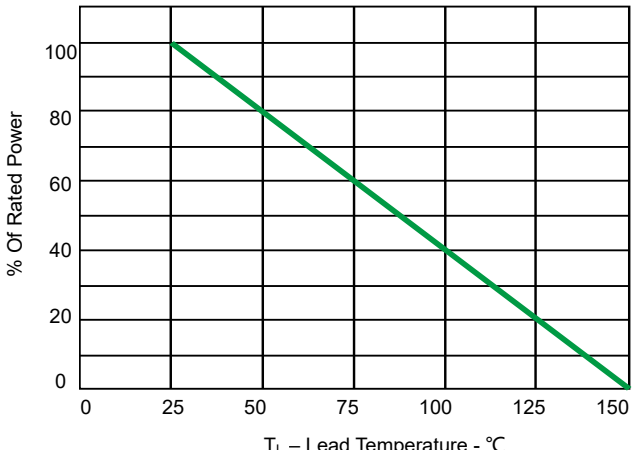


Fig 2.Power Derating Curve

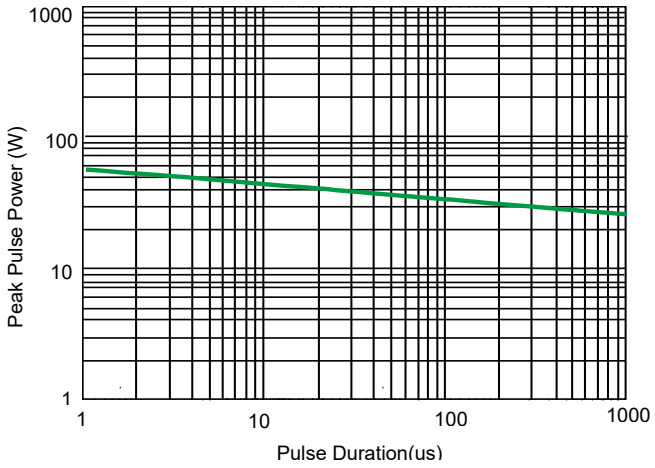


Fig 3.Non-Repetitive Peak Pulse Power vs. Pulse time

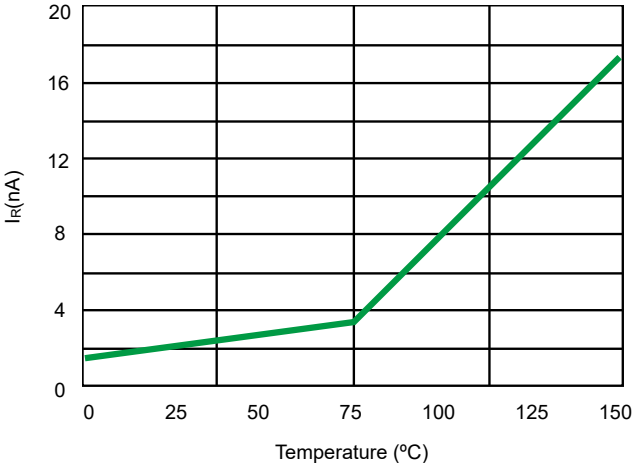


Fig 4.Typical Leakage Current vs. Temperature

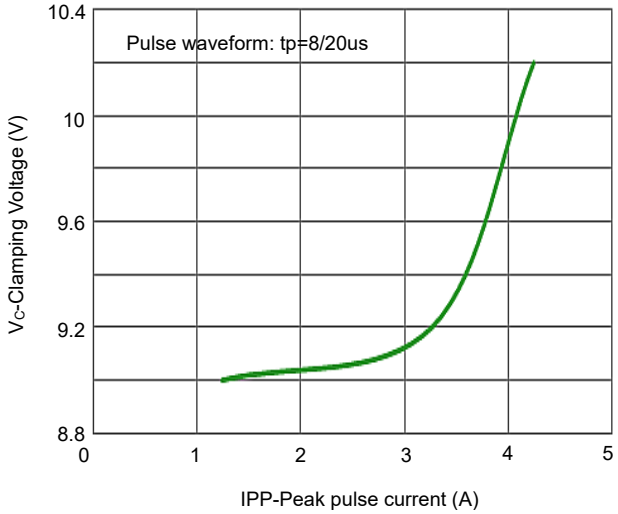


Fig 5. Clamping voltage vs. Peak pulse current

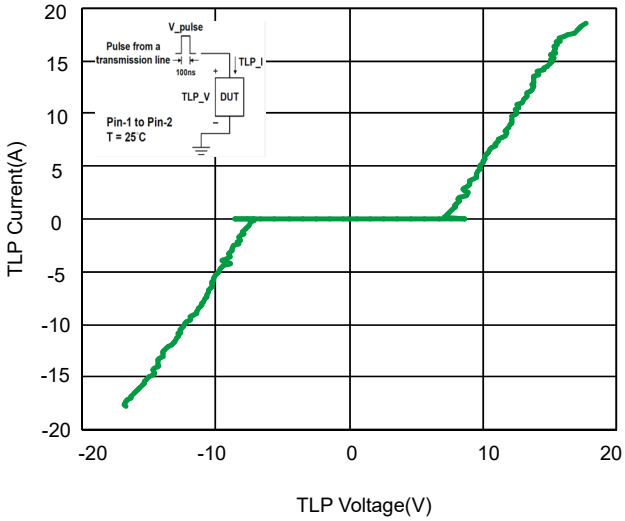


Fig 6. TLP Measurement

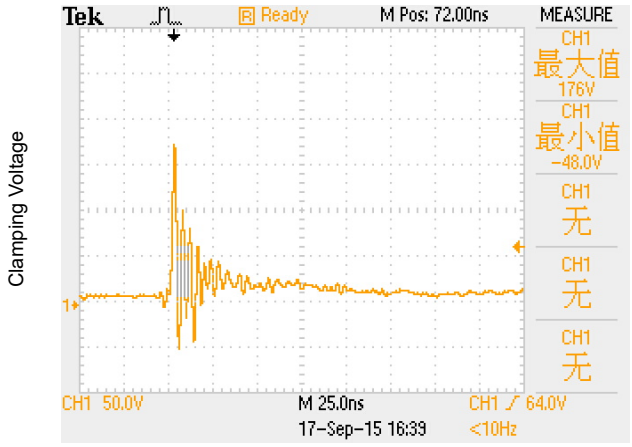
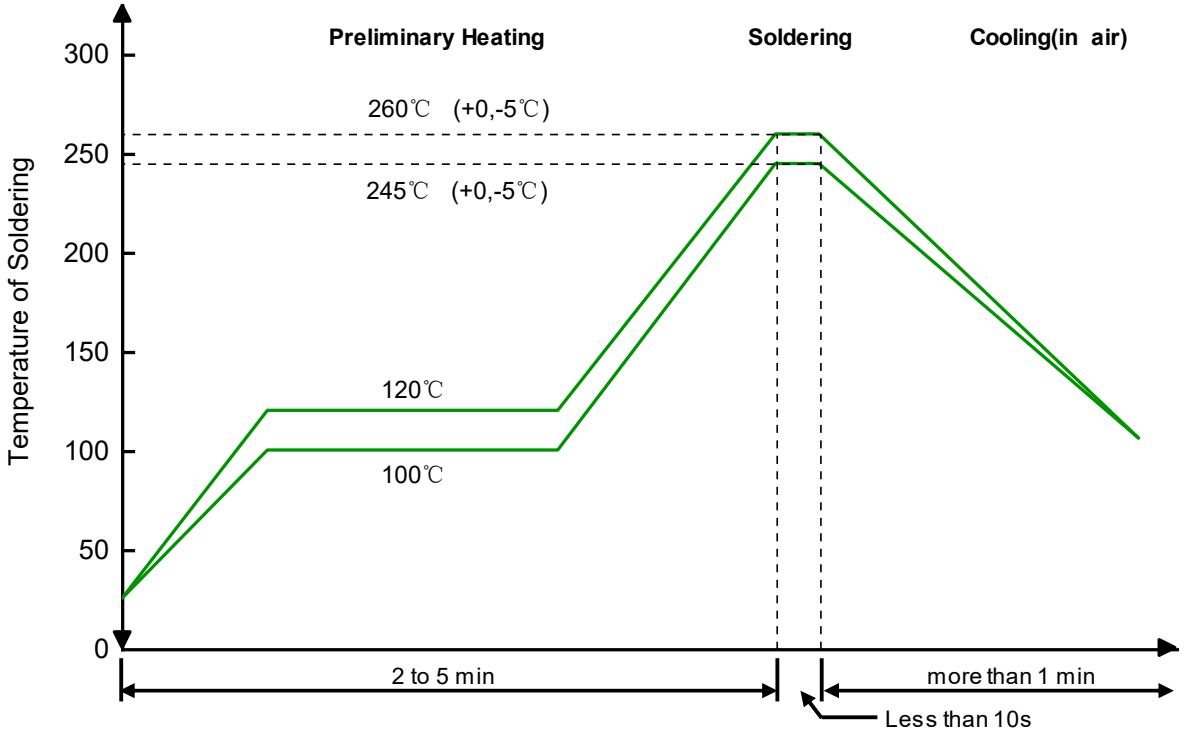


Fig 7. (8kV contact discharge per IEC61000-4-2)

Solder Reflow Recommendation



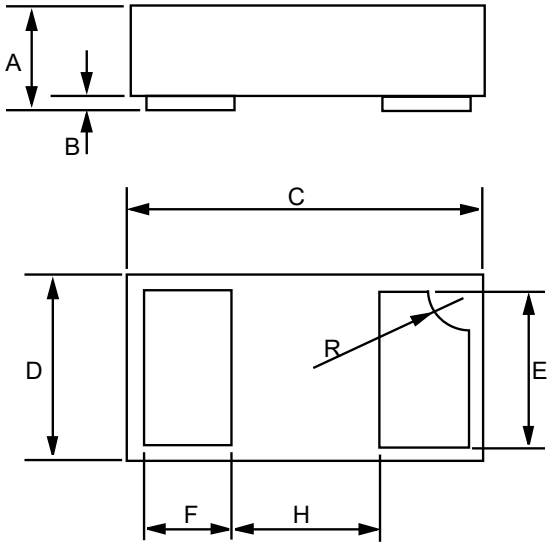
Remark: Pb free for 260℃; Pb for 245℃.

PCB Design

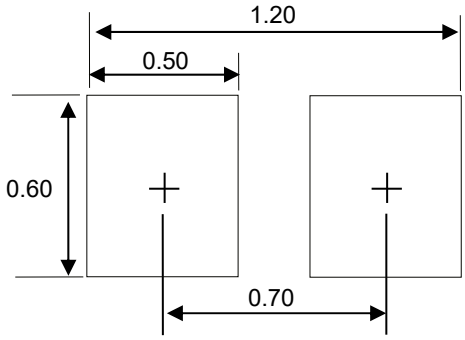
For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

Product dimension (DFN1006-2L)



Dim	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.013	0.020	0.34	0.498
B	0.000	0.002	0.00	0.05
C	0.037	0.043	0.95	1.080
D	0.022	0.027	0.55	0.680
E	0.016	0.024	0.40	0.60
F	0.008	0.012	0.20	0.30
H	0.015Typ.		0.40Typ.	
R	0.001	0.005	0.05	0.15



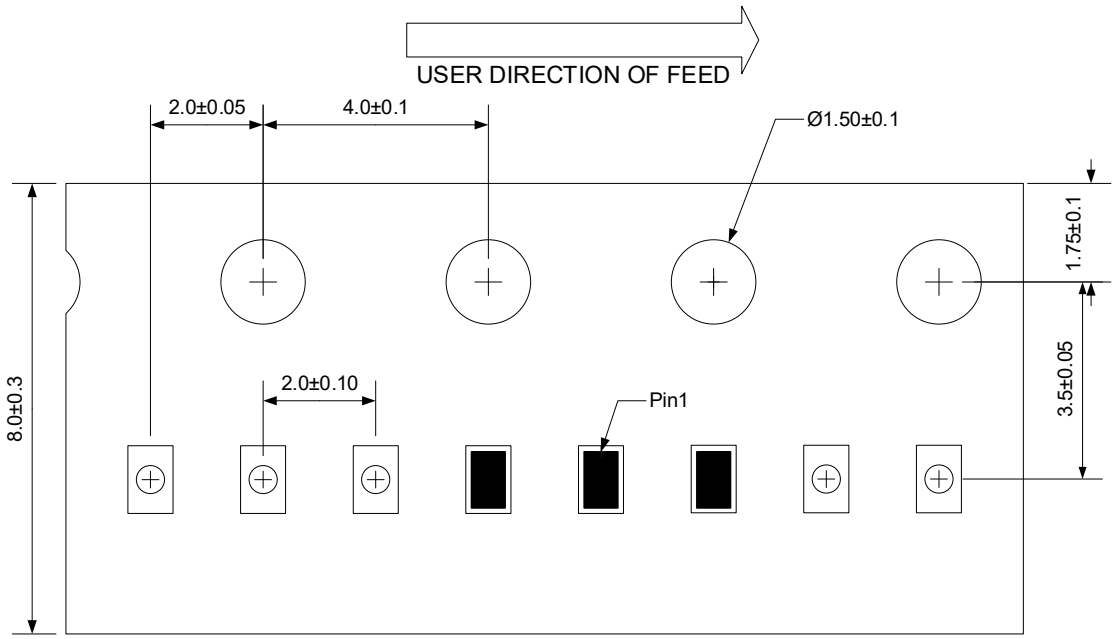
Unit:mm

Suggested PCB Layout

Ordering information

Device	Package	Reel	Shipping
PESDMC2FD5VB	DFN1006-2L (Pb-Free)	7"	10000 / Tape & Reel

Load with information



Unit:mm

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