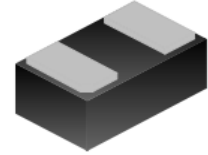


Description

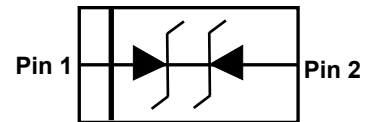
The PESDHC2FD5VBH protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, low operating voltage. It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.



DFN1006-2L(Bottom View)

Feature

- 300W peak pulse power per line ($t_P = 8/20\mu s$)
- DFN1006-2L package
- Replacement for MLV(0402)
- Bidirectional configurations
- Response time is typically $< 1ns$
- Low clamping voltage
- RoHS compliant
- Transient protection for data lines to
IEC61000-4-2(ESD) $\pm 30KV$ (air), $\pm 30KV$ (contact);
IEC61000-4-4 (EFT) 40A (5/50ns)
IEC61000-4-5 (Surge) 33A (8/20us)



Circuit Diagram

Applications

- Cellular phones
- Portable devices
- Digital cameras
- Power supplies



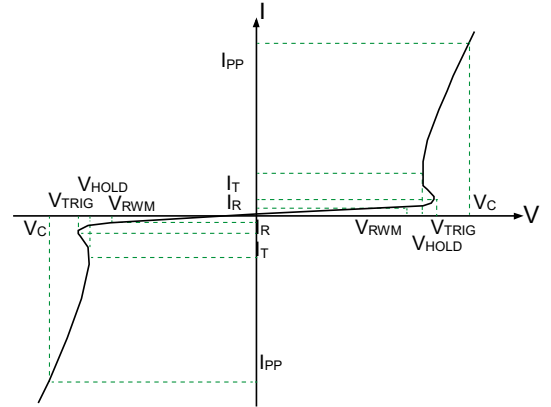
Marking (Top View)

Mechanical Characteristics

- Mounting position: Any
- Qualified max reflow temperature: $260^{\circ}C$
- Device meets MSL 1 requirements
- DFN1006-2L without plating

Electronics Parameter

| Symbol | Parameter |
|------------|-------------------------------------|
| V_{RWM} | Peak Reverse Working Voltage |
| I_R | Reverse Leakage Current @ V_{RWM} |
| V_{TRIG} | Reverse trigger Current |
| V_{HOLD} | Reverse holding voltage |
| I_T | Test Current |
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| P_{PP} | Peak Pulse Power |
| C_J | Junction Capacitance |
| I_F | Forward Current |
| V_F | Forward Voltage @ I_F |



Electrical characteristics per line@25°C (unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|-----------|--------------------------------|------|------|------|---------|
| Peak Reverse Working Voltage(PIN1~PIN2) | V_{RWM} | | | | 5 | V |
| Breakdown Voltage(PIN1~PIN2) | V_{BR} | $I_i=1mA$ | 5.4 | 5.75 | 6.5 | V |
| Reverse Leakage Current(PIN1~PIN2) | I_R | $V_{RWM} = 5V T=25^{\circ}C$ | | | 1.0 | μA |
| Breakdown Voltage (PIN2~PIN1) | V_{BR} | $I_i=1mA$ | 4.6 | 4.85 | 5.5 | V |
| Reverse Leakage Current(PIN2~PIN1) | I_R | $V_{RWM} = 4.5V T=25^{\circ}C$ | | | 1.0 | μA |
| Clamping Voltage(PIN1~PIN2) | V_C | $I_{PP}=1A, t_p=8/20\mu s$ | | 6 | 8 | V |
| Clamping Voltage(PIN1~PIN2) | V_C | $I_{PP}=15A, t_p=8/20\mu s$ | | 7.2 | 9 | V |
| Clamping Voltage(PIN1~PIN2) | V_C | $I_{PP}=33A, t_p=8/20\mu s$ | | 9.5 | 11 | V |
| Junction Capacitance | C_j | $V_R=0V f = 1MHz$ | 70 | 80 | 90 | pF |

Absolute maximum rating@25°C

| Rating | Symbol | Value | Units |
|--------------------------------------|-----------|------------|-------------|
| Peak Pulse Power ($t_p=8/20\mu s$) | P_{pp} | 300 | W |
| Operating Temperature | T_J | -55 to 150 | $^{\circ}C$ |
| Storage Temperature | T_{STG} | -55 to 150 | $^{\circ}C$ |

Typical Characteristics

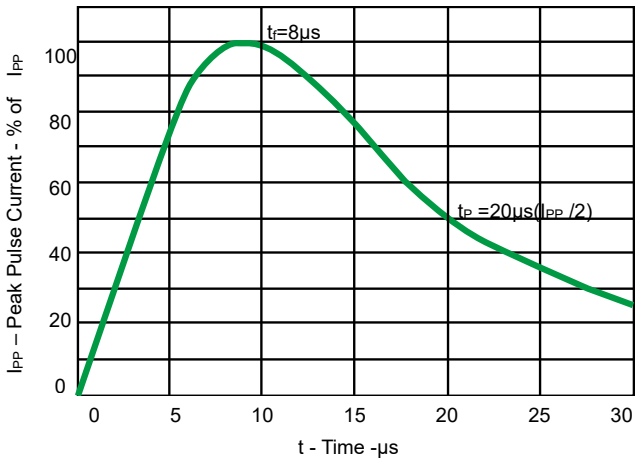


Fig 1. Pulse Waveform

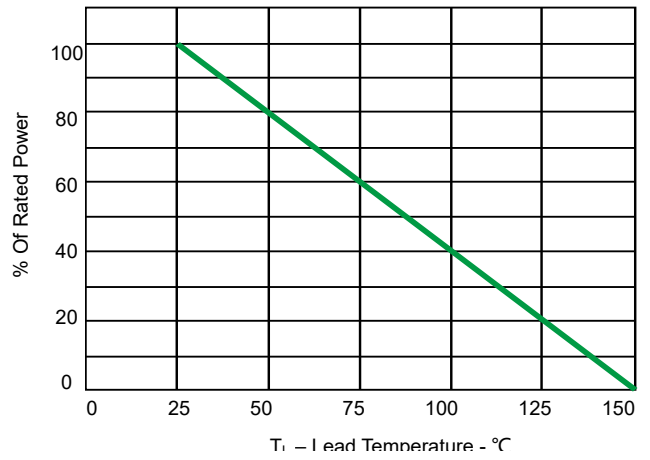


Fig 2. Power Derating Curve

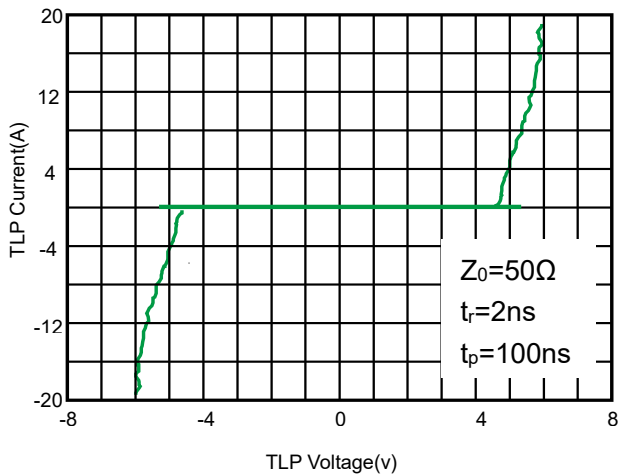


Fig 3. TLP Measurement

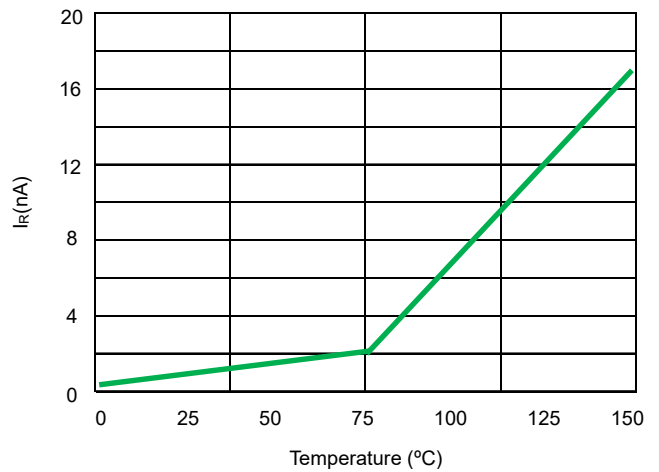


Fig 4. Typical Leakage Current vs. Temperature

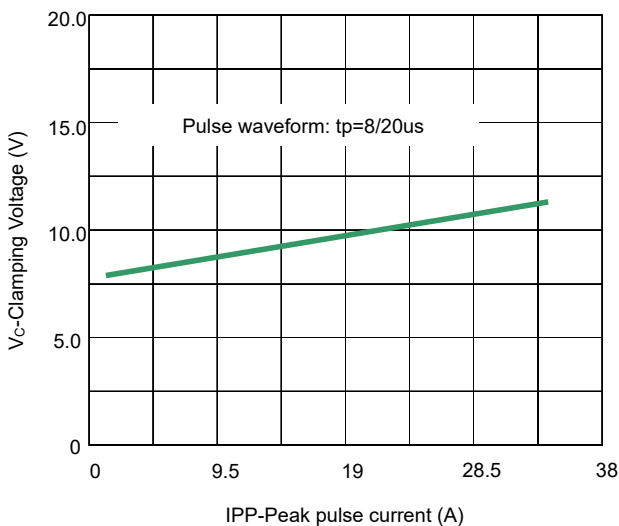


Fig 5. Clamping voltage vs. Peak pulse current

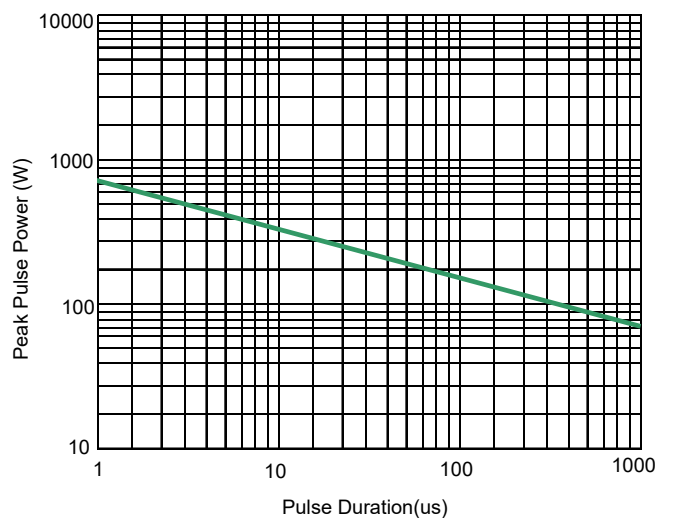


Fig 6. Non-Repetitive Peak Pulse Power vs. Pulse time

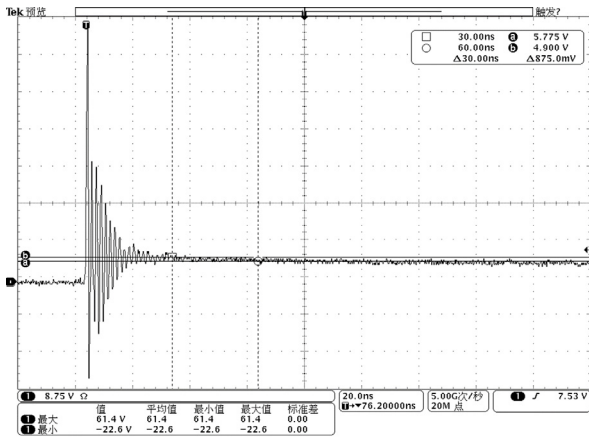


Fig 7. Clamping Voltage at IEC61000-4-2
+8kV Pulse Waveform

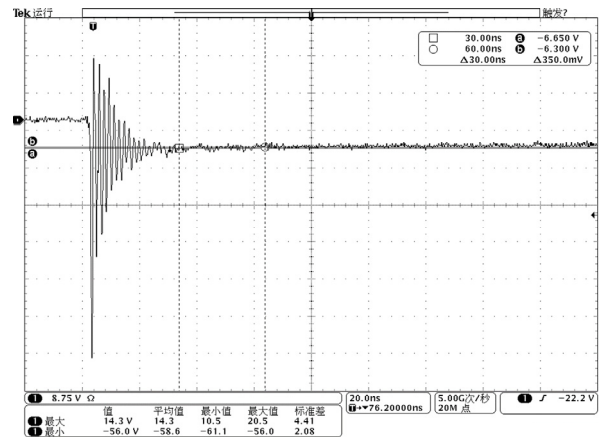
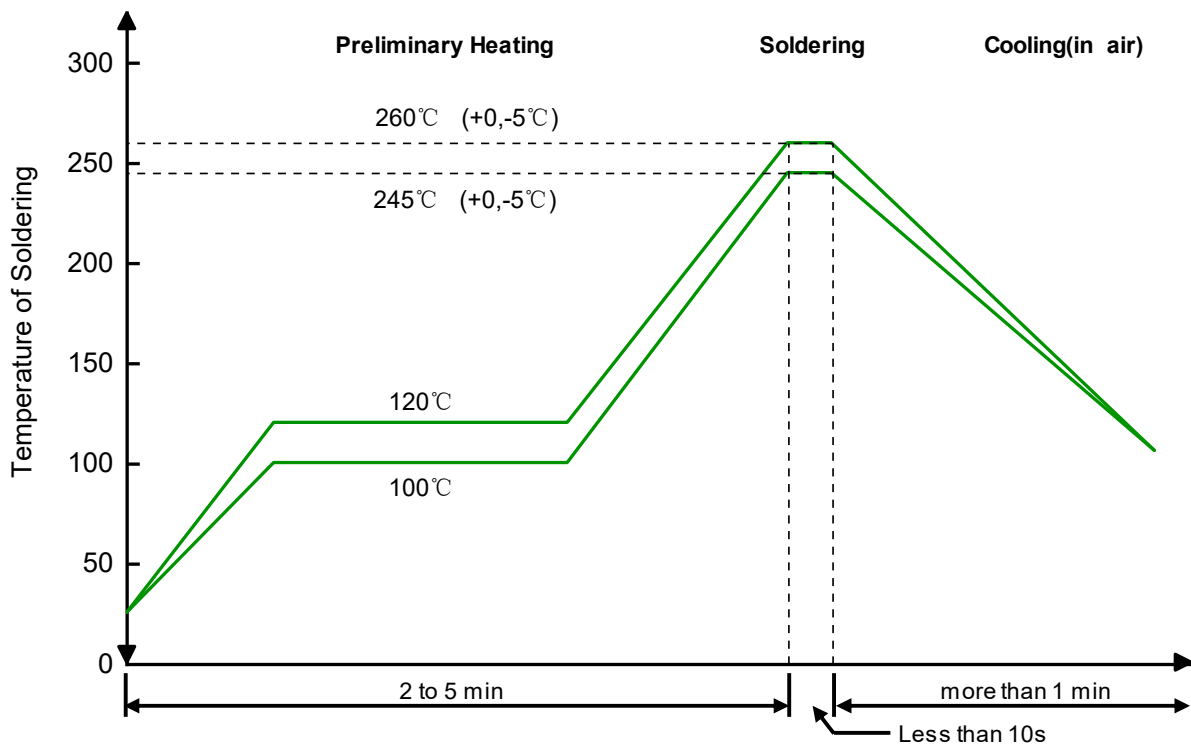


Fig 8. Clamping Voltage at IEC61000-4-2
-8kV Pulse Waveform

Solder Reflow Recommendation



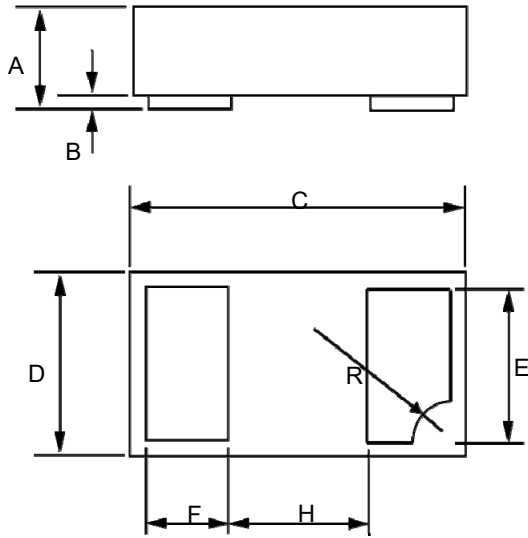
Remark: Pb free for 260°C; Pb for 245°C.

PCB Design

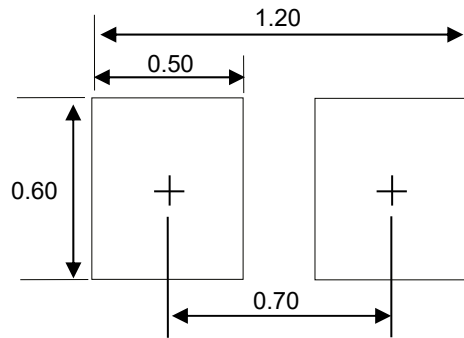
For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

Product dimension (DFN1006-2L)



| Dim | Inches | | Millimeters | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.013 | 0.020 | 0.34 | 0.498 |
| B | 0.000 | 0.002 | 0.00 | 0.05 |
| C | 0.037 | 0.043 | 0.95 | 1.080 |
| D | 0.022 | 0.027 | 0.55 | 0.68 |
| E | 0.016 | 0.024 | 0.40 | 0.60 |
| F | 0.008 | 0.012 | 0.20 | 0.30 |
| H | 0.015Typ. | | 0.40Typ. | |
| R | 0.001 | 0.005 | 0.05 | 0.15 |



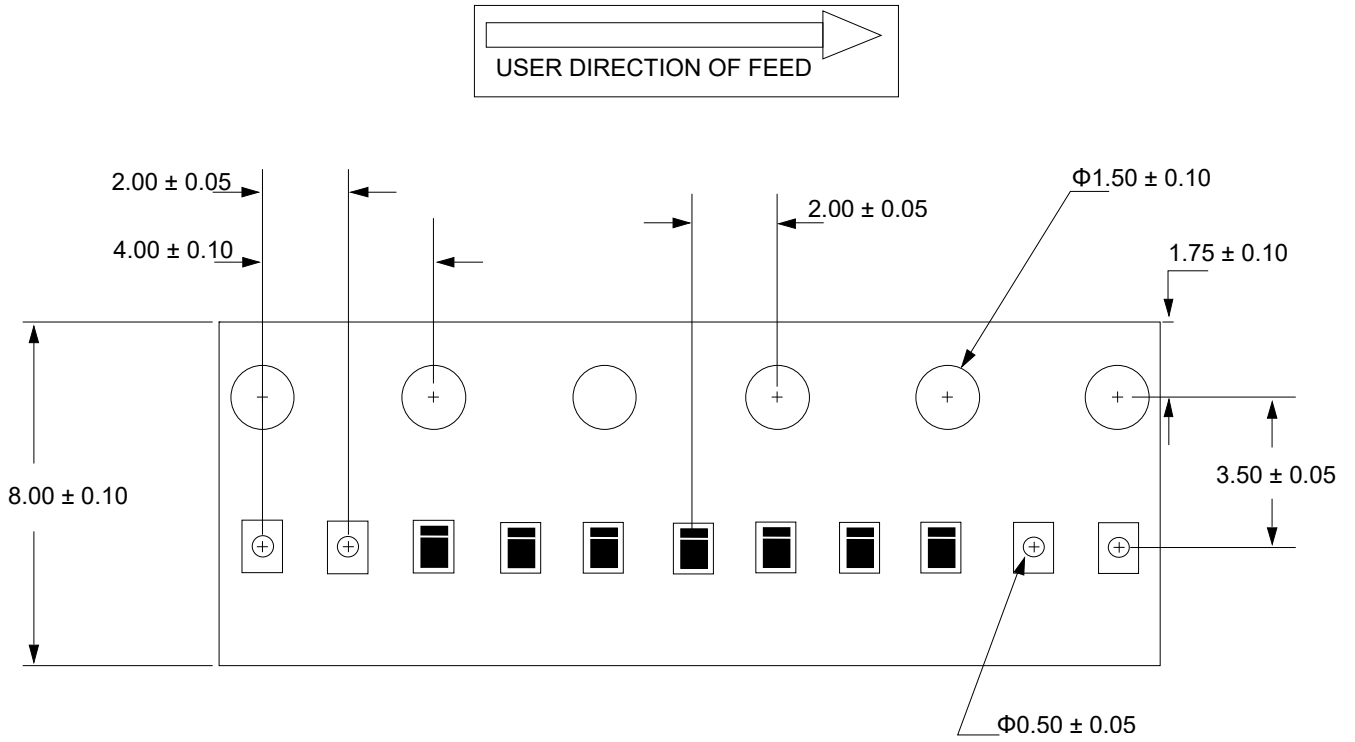
Suggested PCB Layout

Unit:mm

Ordering information


| Device | Package | Reel | Shipping |
|---------------|----------------------|------|---------------------|
| PESDHC2FD5VBH | DFN1006-2L (Pb-Free) | 7" | 10000 / Tape & Reel |

Load with information



Unit: mm


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