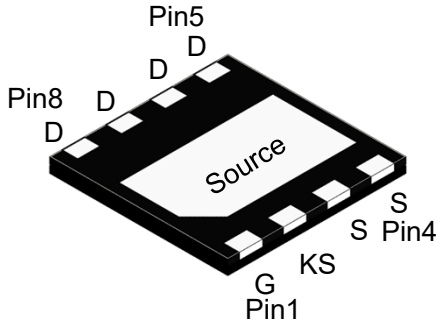
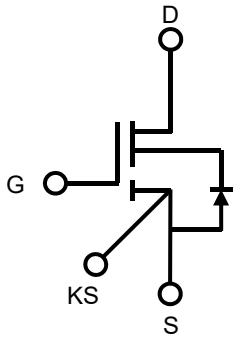
700V Enhancement-mode GaN Transistor

Description

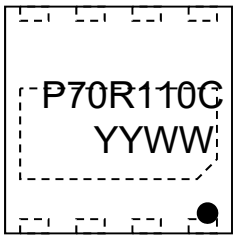
700V Normally-OFF GaN			
V_{DS}(V)	$R_{DS(on)}$(mΩ)	I_{DS}(A)	Q_G(nC)
700	110	20	7.9



Bottom View



Circuit Diagram



Pin4 Pin1

Marking (Top View)

Feature

- Normally-off device combines high voltage GaN HEMT and low voltage silicon MOSFET
- Normally off power switch
- Low reverse-recovery charge
- High switching frequency
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- RoHS compliant and Halogen-free
- Package:DFN8*8-8L

Applications

- Fast charger
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

Absolute maximum rating@25℃

Rating		Symbol	Value	Units
Drain-Source Voltage		V_{DS}	700	V
Drain-Source Voltage-transient[1)]		$V_{(TR)DSS}$	800	V
Gate-Source Voltage		V_{GS}	-20 to +20	V
Drain Current-Continuous[2)]	T_C =25℃	I_D	20	A
	T_C =125℃		9	A
Pulse Drain Current (pulse width: 100μs)		I_{DM}	35	A
Maximum Power Dissipation		P_D	90	W
Junction and Storage Temperature Range		T_J,T_S	-55~+150	℃

Notes:
1. In off-state, spike duty cycle D<0.01, spike duration <1μs
2. For increased stability at high current operation.

Thermal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Thermal Resistance, Junction - Case	$R_{\theta JC}$	-	-	1.4	℃/W

Electrical characteristics per line@25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V	700	-	-	V
Total Drain Leakage Current	I_{DSS}	V_{DS}= 700V,V_{GS}= 0V,T_J=25℃	-	-	10	μA
		V_{DS}= 700V,V_{GS}= 0V, T_J=150℃	-	-	100	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D= 1mA	3.0	4.0	4.8	V
Gate Threshold Voltage Temperature Coefficient	$\triangle V_{GS(th)}/T_J$		-	-7	-	mV/℃
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ±20V	-	-	±100	nA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D= 1A	-	110	150	mΩ
		V_{GS}= 10V, I_D= 1A, T_J=150℃	-	230	-	
Input Capacitance	C_{iss}	V_{DS}= 400V,V_{GS}= 0V, f= 1MHz	-	293	-	pF
Output Capacitance	C_{oss}		-	17	-	
Reverse Transfer Capacitance	C_{rss}		-	3.74	-	
Output Charge	Q_{oss}	V_{GS} =0V, V_{DS} =0V to 400V, f= 1MHz	-	22.2	-	nC
Total Gate Charge	Q_g	V_{GS}=0 to 10V, V_{DS}=400V, I_D=1A	-	7.9	-	nC
Gate-Source Charge	Q_{gs}		-	2.31	-	
Gate-Drain Charge	Q_{gd}		-	1.65	-	
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=400V, V_{GS}=0V to 10V, I_D=2.1A, $R_{G-on(ext)}$=6.8Ω, $R_{G-off(ext)}$=2.2Ω, L=250μH	-	3.2	-	ns
Turn-on Rise Time	t_r		-	5.5	-	
Turn-Off Delay Time	$t_{d(off)}$		-	7.4	-	
Turn-Off Fall Time	t_f		-	27	-	
Reverse Device Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}= 0V,I_{SD}= 10A	-	2.1	-	V
Reverse Recovery Time	t_{rr}	I_F=10A, V_{DD}=400V, dI_F/dt=165A/μs	-	14	-	ns
Reverse Recovery Charge	Q_{rr}		-	6.5	-	nC

Typical Characteristics

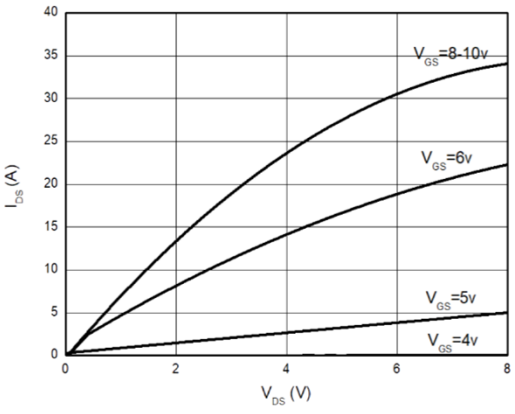


Figure 1. Typical Output Characteristics T_J=25°C

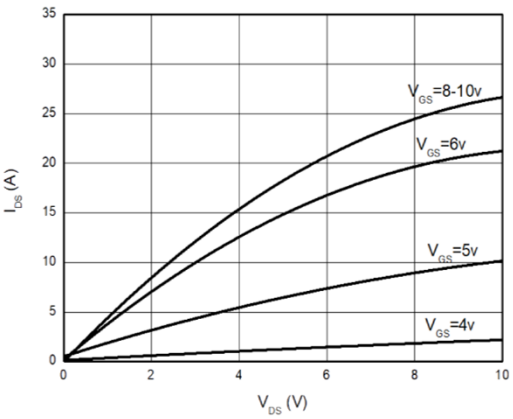


Figure 2. Typical Output Characteristics T_J=125°C

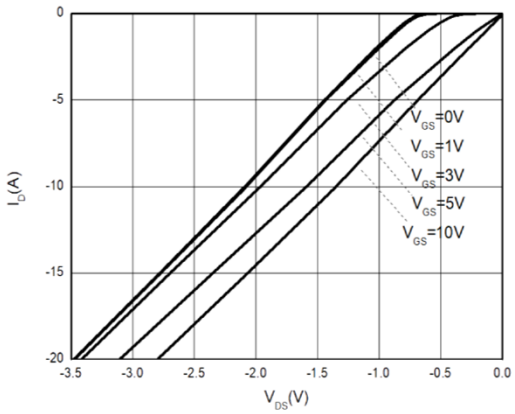


Figure 3. Channel Reverse Characteristics T_J=25°C

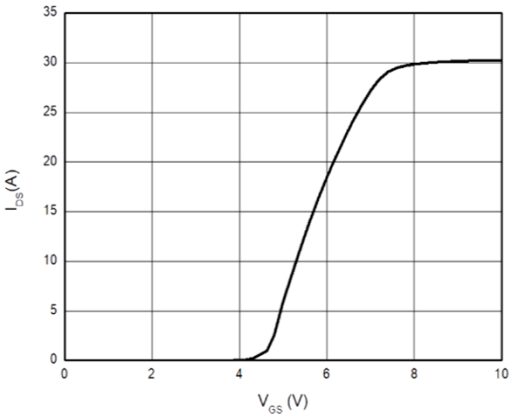


Figure 4. Typical Transfer Characteristics (V_{DS}=10V)

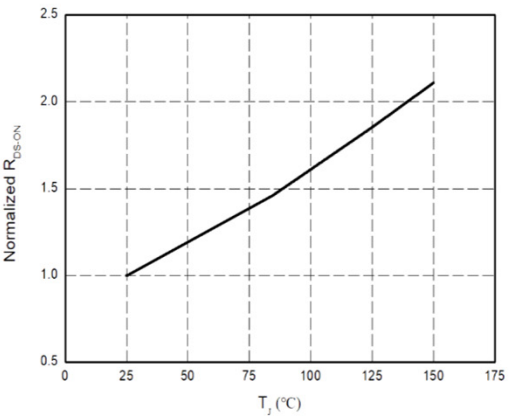


Figure 5. Normalized On-resistance

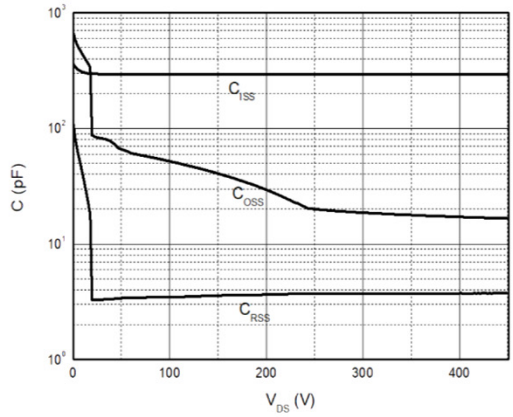


Figure 6. Typical Capacitance (f=1MHz)

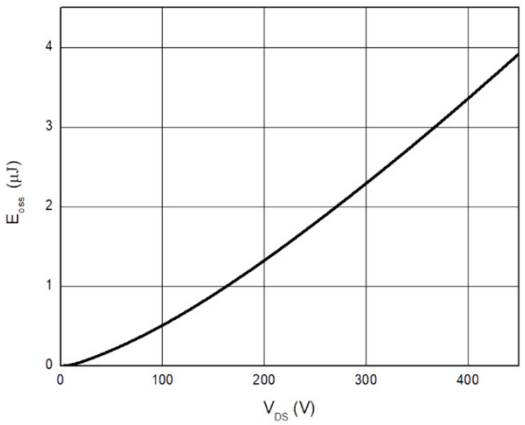


Figure 7. Typical C_{OSS} Stored Energy

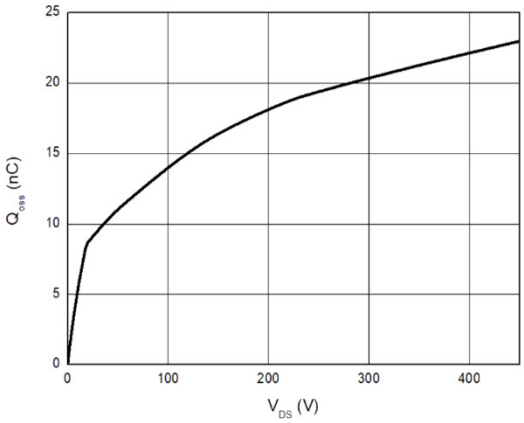


Figure 8. Typical Q_{OSS}

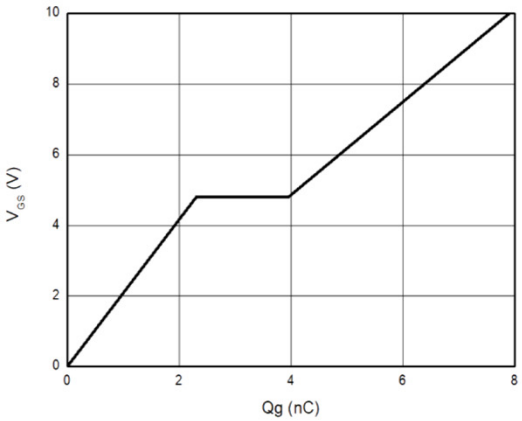


Figure 9. Typical Gate Charge (V_{DS}=400V, I_D=1A)

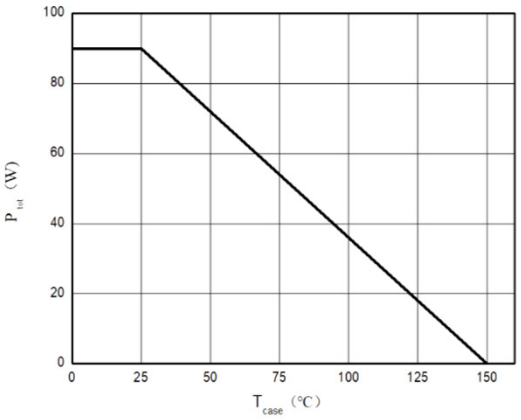
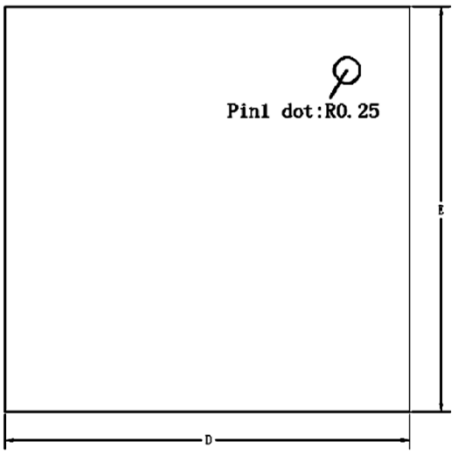


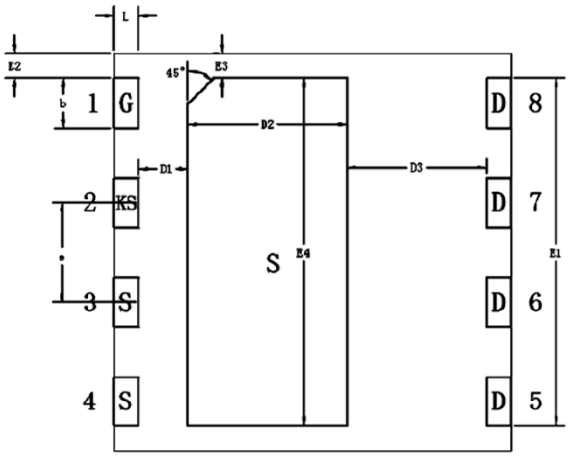
Figure 10. Power Dissipation

Product Dimension (DFN8*8-8L)

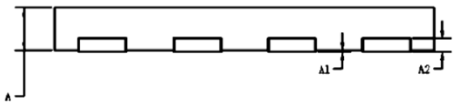
Top view



Bottom view



Side view(left/right)



Dim	Millimeters		Inches		Dim	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	1.05	1.15	0.041	0.045	E1	6.90	7.10	0.272	0.280
A1	0.00	0.05	0.000	0.002	E2	0.40	0.60	0.016	0.024
A2	0.203 Ref.		0.008 Ref.		E3	0.40	0.60	0.016	0.024
D	7.90	8.10	0.311	0.319	E4	6.90	7.10	0.272	0.280
E	7.90	8.10	0.311	0.319	b	0.90	1.10	0.035	0.043
D1	0.90	1.10	0.035	0.043	e	1.90	2.10	0.075	0.083
D2	3.10	3.30	0.122	0.130	L	0.40	0.60	0.016	0.024
D3	2.70	2.90	0.106	0.114					

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