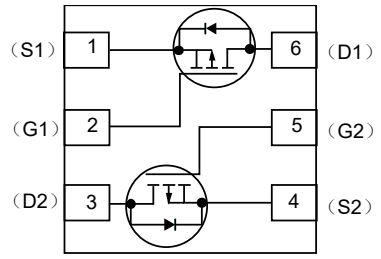
Description

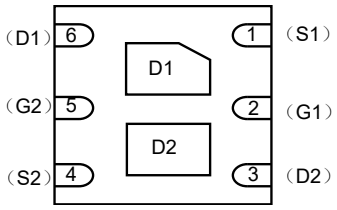
The enhancement mode MOS is extremely high density cell and low on-resistance.

MOSFET Product Summary		
V_{DS}(V)	$R_{DS(on)}$(mΩ)	I_D(A)
-20	110 @ V_{GS}=-4.5V	-3

Internal structure



Bottom View



Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current- Continuous	I_D	-3	A
Drain Current- Pulsed	I_{DM}	-10	A
Total Power Dissipation	P_D	1	W
Operating and Storage Junction Temperature Range	T_J,T_{STG}	-55 to +150	℃

Thermal Characteristics

Parameter	Symbol	Max.	Units
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	℃/W

Electrical characteristics per line@25℃(unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =-250μA,V_{GS}=0V	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =-20V,V_{GS}=0V	-	-	-1.0	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=±12V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.4	-0.7	-1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D =-3A	-	64	110	mΩ
		V_{GS}=-2.5V, I_D =-2A,	-	89	140	mΩ
Forward Trans conductance	g_{FS}	V_{DS}=-5V, I_D =-2.8A	-	9.5	-	S
Total Gate Charge	Qg	I_D =-3A, V_{DS} =-10V, V_{GS} =-2.5V	-	3.3	12	nC
Gate-to-Source Charge	Qgs		-	0.7		
Gate-to-Drain(Miller) Charge	Qgd		-	1.3		
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS} =-10V, f=1MHz	-	405		pF
Output Capacitance	C_{DSS}		-	75		pF
Reverse Transfer Capacitance	C_{RSS}		-	55		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=-10V, I_D =-1A, V_{GS}=-4.5V , R_{GEN}=10Ω,	-	11		ns
Rise Time	t_r		-	35		
Turn-Off Delay Time	$t_{d(off)}$		-	30		
Fall Time	t_f		-	10		
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=-1.3A			-1.2	V
Diode Forward Current	I_S				-1.3	A

Typical Characteristics

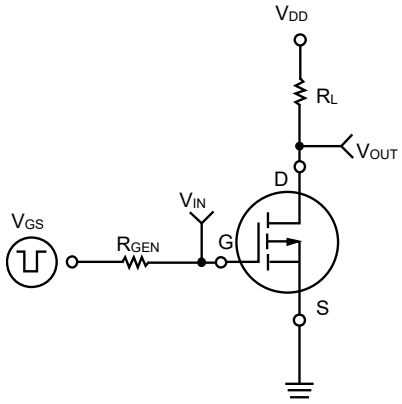


Figure 1. Switching Test Circuit

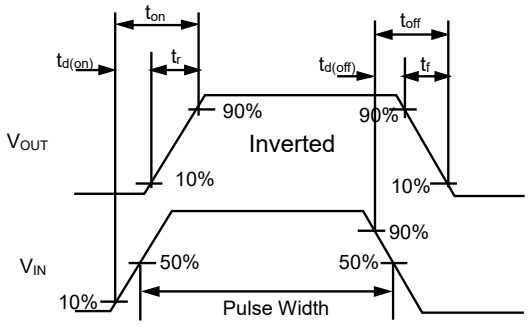


Figure 2. Switching Waveforms

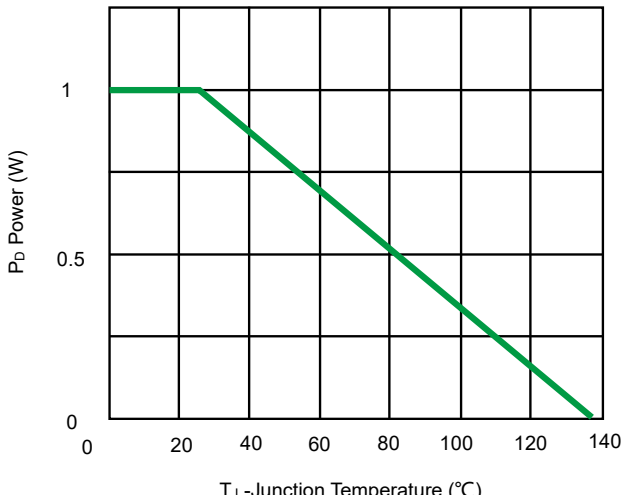


Fig 3. Power Dissipation

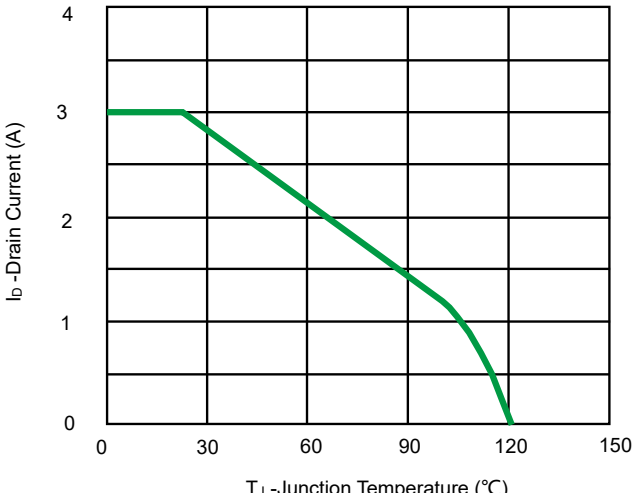


Fig 4. Drain Current

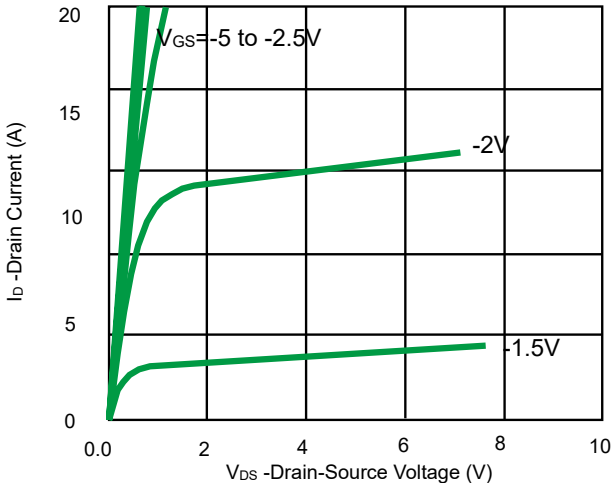


Fig 5. Output Characteristics

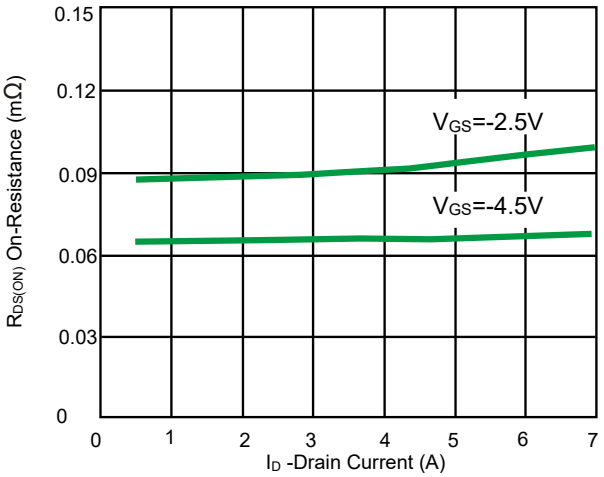


Fig 6. Drain-Source On-Resistance

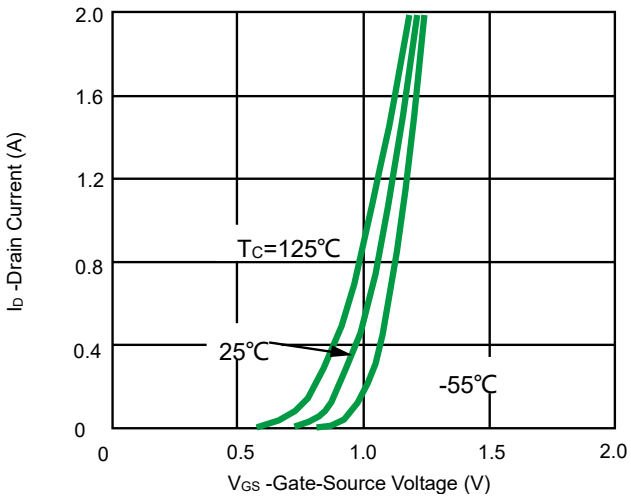


Fig 7. Transfer Characteristics

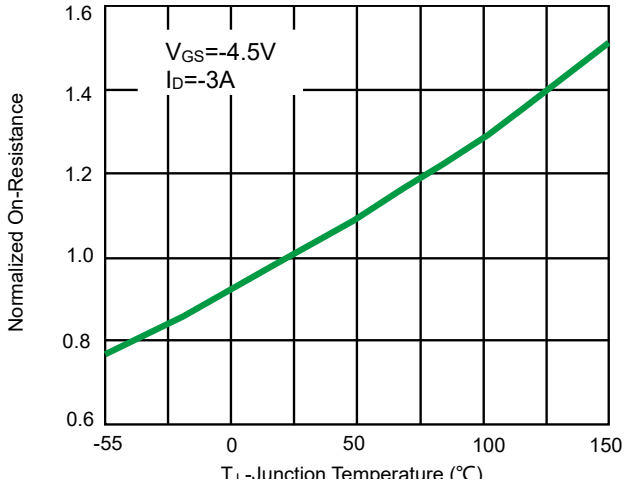


Fig 8. Drain-Source On-Resistance

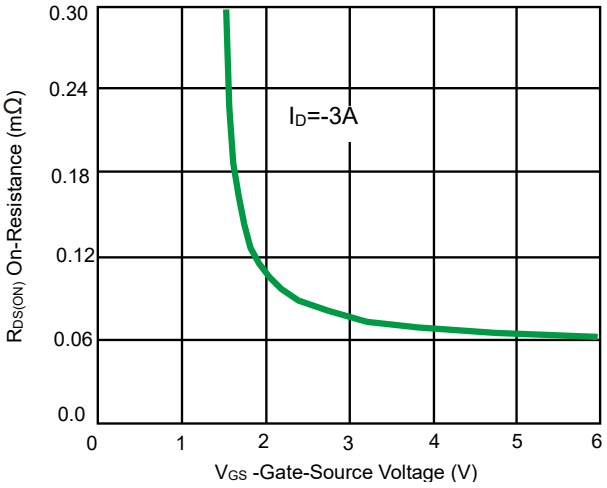


Fig 9. $R_{DS(ON)}$ vs. V_{GS}

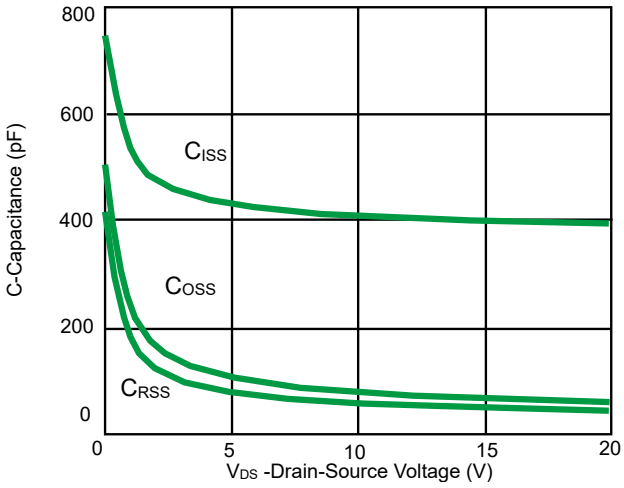


Fig 10. Capacitance vs. V_{DS}

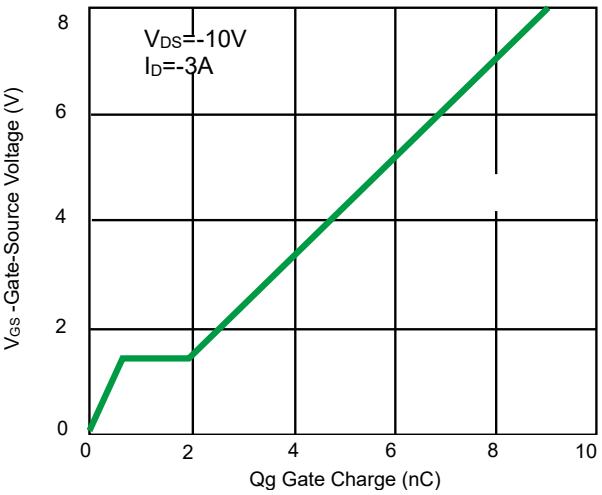


Fig 11. Gate Charge

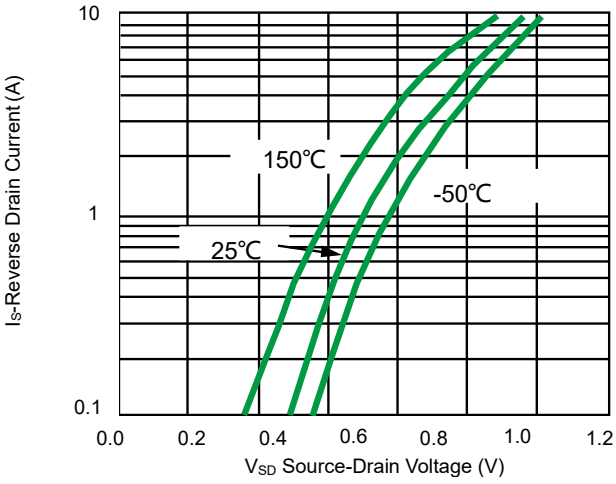


Fig 12. Source-Drain Diode Forward

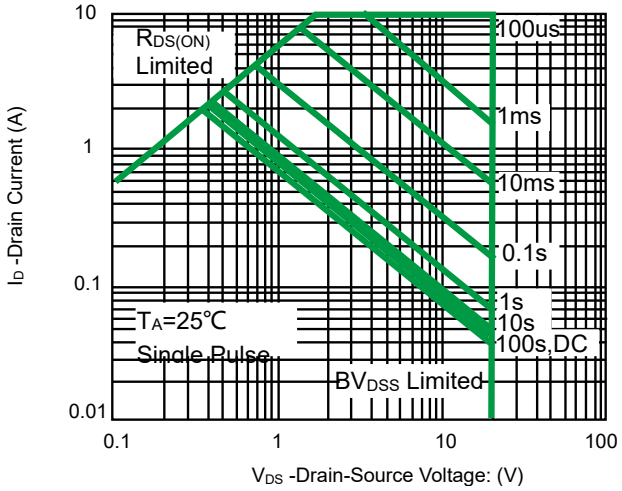


Figure 13. Safe Operation Area

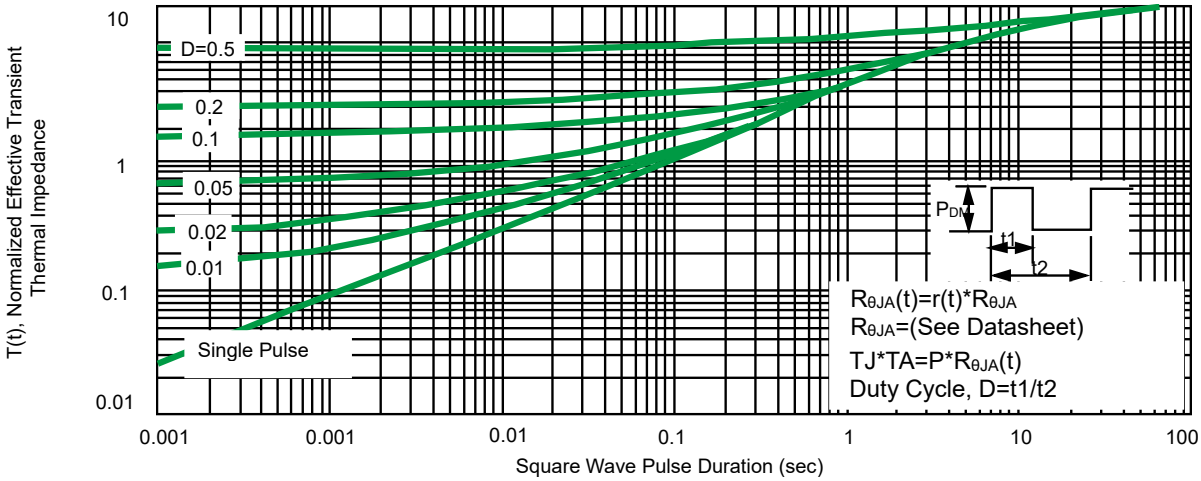
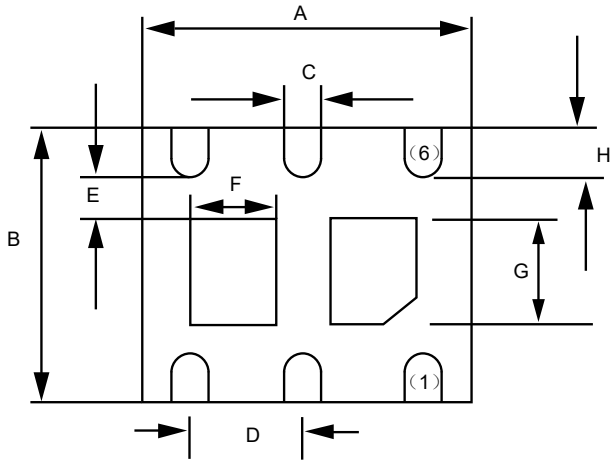
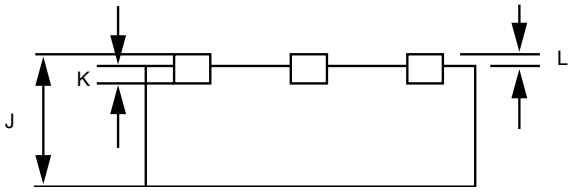


Fig 14.Normalized Maximum Transient Thermal Impedance

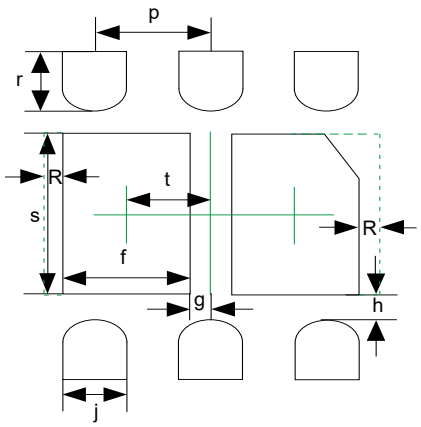
Product dimension (DFN2020-6L)



Bottom View



Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	1.924	2.076	0.076	0.082
B	1.924	2.076	0.076	0.082
C	0.250	0.350	0.010	0.014
D	0.650（typ.）		0.026（typ.）	
E	0.200 MIN.		0.008 MIN.	
F	0．520	0.720	0.020	0.028
G	0.900	1.100	0.035	0.043
H	0.174	0.326	0.007	0.013
J	0.700	0.800	0.028	0.031
K	0.206 REF		0.206 REF	
L	0.203 REF		0.203 REF	



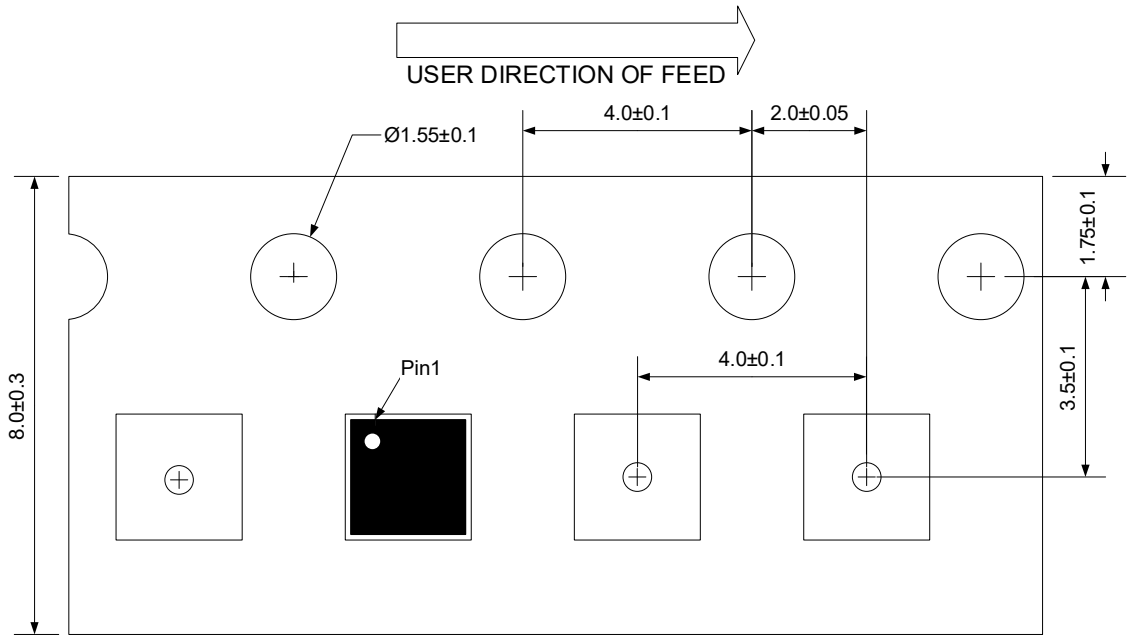
If there is enough place in PCB. It can be mounted with copper along the dotted line in order to optimize thermal design.

Dim	Millimeters	
	MIN	MAX
p	0.60	0.70
r	0.40	0.50
s	1.05	1.15
t	0.42	0.52
f	0.67	0.77
g	0.06	0.16
h	0.1	0.2
j	0.35	0.45
R	0.1	0.2

Ordering information

Device	Package	Shipping
PDPM6N20V3	DFN2020-6L	3000 / Tape & Reel

Load with information



Unit:mm

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